

WET CLEANING METHOD TO ELIMINATE COPPER CORROSION

FIELD OF THE INVENTION

[0001] The present invention relates, most generally, to the manufacture of semiconductor devices. More particularly, the present invention relates to a semiconductor substrate cleaning method that prevents copper corrosion.

BACKGROUND

[0002] Copper is favored as a conductive material used in interconnect features in advanced, high-speed semiconductor devices. Damascene and dual damascene interconnect technology is advantageously used to provide planarized interconnect structures in advanced semiconductor manufacturing technologies. In processing operations used to form damascene, dual damascene and other openings, a dielectric layer is etched to expose a protective layer or etch stop layer. The exposed layer may be disposed directly between a subjacent copper-containing conductive material and the environment. A shortcoming of the use of copper is that copper is susceptible to corrosion when exposed to the environment.

[0003] Dielectric etching operations use a photoresist film as an etch mask. After the conclusion of the etching operation used to form the damascene, dual damascene or other openings in the dielectric layer, a sequence of cleaning operations is used to remove the photoresist film and other undesired by-products and contaminants generated during the etching operation, and to clean and dry the semiconductor substrate. The phenomenon of copper corrosion could result during these cleaning operations or subsequent to the cleaning operations as a result of the condition of the substrate.

[0004] According to conventional processing methods, the post-etch cleaning operation typically includes a DI water cleaning step in which the semiconductor substrate is rotated at a relatively high spin speed, such as 500-1000 rpm. It has been found that the DI water cleaning step introduces a high potential gradient across the semiconductor substrate due to electrostatic charge build-up produced by friction

between the semiconductor substrate surface and the DI water. This potential gradient induces breakdown of dielectric materials such as etch stop layers or other protective layers which separate a copper containing conductive material disposed beneath such layer, from the environment after the layer is exposed during the dielectric etching operation. The breakdown of such a layer exposes copper and leads to copper corrosion. The potential gradient also creates a battery circuit that, through galvanic effect, also causes copper corrosion. Copper corrosion causes device failure or at least device functionality problems.

[0005] It would therefore be desirable to provide a post-etch semiconductor substrate cleaning operation that effectively cleans the semiconductor substrate and does not cause copper corrosion.

SUMMARY OF THE INVENTION

[0006] To address the aforementioned shortcomings of conventional technology and in view of its purposes, the present invention provides a method for effectively cleaning semiconductor substrates that are susceptible to copper corrosion, while maintaining the integrity of the copper features and preventing copper corrosion.

[0007] In one embodiment, the present invention provides a method for reducing copper corrosion in a semiconductor device. The method includes providing a semiconductor substrate that has a copper-containing conductive material and a film directly interposed between the copper containing conductive material and the environment. The method further provides cleaning the semiconductor substrate including using a DI water clean operation that includes rotating the semiconductor substrate at a spin speed no greater than 350 rpm.

[0008] The method of the present invention may be used in various semiconductor substrate cleaning operations including after the dielectric etching operations used to form damascene or dual damascene openings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The present invention is best understood from the following detailed description when read in conjunction with the accompanying drawings. It is emphasized that, according to common practice, the various features of the drawings are not necessarily to scale. On the contrary, the dimensions of the various features are arbitrarily expanded or reduced for clarity. Like numerals denote like features throughout the specification and drawings. Included are the following figures:

[0010] Figure 1 is a cross sectional view showing an exemplary etched structure according to the PRIOR ART and which may be cleaned according to the method of the present invention; and

[0011] Figure 2 is a cross sectional view showing another exemplary etched structure according to the PRIOR ART and which may be cleaned according to the method of the present invention

DETAILED DESCRIPTION

[0012] The present invention provides a semiconductor substrate cleaning method that prevents copper corrosion. The cleaning method includes a DI (deionized) water cleaning operation in which the semiconductor substrate, alternatively referred to as a "wafer", is rotated at a speed of no greater than 350 rpm. As will be discussed, the cleaning method of the present invention may include multiple distinct cleaning operations or steps.

[0013] The wafer cleaning method of the present invention may be used at various stages during the formation of semiconductor devices on the wafer. A particularly advantageous application of the present invention is a cleaning operation used to clean a wafer with a copper-containing conductive material formed thereon and a film directly interposed between the copper containing conductive material and the environment. Such a structure may be produced after an etching operation. Figures 1 and 2 are each cross-sectional views of exemplary conventional structures used to produce semiconductor devices and which find particular advantage in being cleaned by the method of the present invention. In Figures 1 and 2, Cu-containing conductive

material 2 is formed over a semiconductor substrate (not shown). Cu-containing conductive material 2 may be a copper film used as an interconnect wire and it may be substantially pure copper in an exemplary embodiment, but other Cu-containing conductive materials such as copper alloys, may be used in other exemplary
5 embodiments. Film 6 is formed over surface 4 of Cu-containing conductive material 2 and is directly interposed between Cu-containing conductive material 2 and the environment 20 in locations where film 6 is not covered by dielectric layer 10. As such, exposed portion 16 of film 6 is particularly sensitive to breakdown due to potential issues discussed above and the breakdown of portion 16 of film 6 exposes portions of
10 Cu-containing conductive material 2 to environment 20 and leads to copper corrosion. In Figure 1 opening 12 is formed in dielectric layer 10 to expose surface 8 of film 6. In Figure 2, two-tiered opening 22 is formed in dielectric layer 10 and exposes surface 8 of film 6.

[0014] Figures 1 and 2 may each represent structures following an etching
15 operation in which photoresist mask 14 was used to mask dielectric layer 10 and form the respective opening. In this manner, film 6 may serve as an etch-stop layer. Film 6 may be formed of materials such as SiN, SiC, SiOC, SiCN or various other suitable films used as etch-stop layers or layers otherwise used to separate or protect a Cu-containing conductive material from the environment. Film 6 may include a thickness
20 within the range of 400-800 angstroms, but other thicknesses may be used in other exemplary embodiments.

[0015] In an exemplary embodiment, the cleaning method of the present invention may be used after one or more of the etch processes in the process sequence used to form a damascene or dual damascene opening in the dielectric film. Figure 1
25 shows an exemplary damascene opening 12 and Figure 2 shows an exemplary dual damascene opening 22. Figure 1 may alternatively represent the first (via etch) step in the process sequence used to form the dual damascene opening 22 shown in Figure 2 and which may be formed after a subsequent trench etching operation. Various dielectric materials may be used as dielectric layer 10 and dielectric layer 10 may
30 represent a single film or a plurality of dielectric films. In one exemplary embodiment,

dielectric layer 10 may be a low-k dielectric material. In one exemplary embodiment, dielectric layer 10 may include at least one layer of carbon-containing material. In another exemplary embodiment, dielectric layer 10 may include at least one layer of fluorine-containing material and in yet another exemplary embodiment, dielectric layer 10 may include at least one layer of nitrogen-containing material. Other dielectric materials may be used in other exemplary embodiments. Various suitable photoresist materials may be used as photoresist 14. Various etching processes and etchant species may be chosen and used to appropriately etch the materials used as dielectric layer 10.

[0016] In an exemplary embodiment, the wet cleaning operation of the present invention may be preceded by any of various suitable dry plasma ashing operations directed at removing photoresist 14.

[0017] The cleaning method of the present invention includes a DI water cleaning operation and may include one or more wet cleaning operations prior to the DI water cleaning operation and one or more cleaning, rinsing, and/or drying operations after the DI water cleaning operation. The various sequences of wet cleaning operations may be performed in-situ and in various wet cleaning tools such as SEZ4300 manufactured by SEZ AG and various wet cleaning tools manufactured by Semitool, Inc. of Kalispell, MT. The cleaning tool may individually rotate the semiconductor substrates, and in an exemplary embodiment, may individually process semiconductor substrates in a single-wafer processing chamber.

[0018] In one exemplary cleaning sequence of the present invention, at least one of an organic solvent clean, an aqueous chemical clean or a DI water/ozone clean may take place in-situ prior to the DI water cleaning operation. In an exemplary embodiment, the organic solvent clean may include a spin speed of 150-800 rpm and may contain fluorine. "Spin speed" is the speed at which the individual semiconductor substrate or wafer is rotated during processing. In an exemplary embodiment, the DI water/ozone clean operation may include a spin speed ranging from 150 to 350 rpm and in an exemplary embodiment the aqueous chemical clean may include a spin speed of 150-350 rpm. Such are intended to be exemplary only and various other cleaning

operations with various spin speeds may be performed in-situ, along with the DI water cleaning operation of the present invention.

[0019] The DI water cleaning operation of the present invention preferably takes place at a spin speed no greater than 350 rpm. In an exemplary embodiment, the spin speed may be greater than 150 rpm and a spin speed of about 200 rpm may be used in one exemplary embodiment. In an exemplary embodiment in which a 300 millimeter wafer is used, the spin speed may range from 180 to 250 rpm and in another exemplary embodiment in which a 200 mm wafer is used, the spin speed may range from 200 to 300 rpm, but other spin speeds may be used in other exemplary embodiments. The duration of the DI water cleaning operation may vary and in one exemplary embodiment the duration of this operation may be two minutes. DI water may be delivered to the surface of the wafer using conventional means. During the DI water cleaning operation, nitrogen and/or air may be the gases of the ambient environment within the region of the tool in which the cleaning operation takes place.

[0020] The DI water cleaning operation may be followed by one or more in-situ further cleaning or rinsing operations. After the cleaning and rinsing operations are concluded, an in-situ drying operation may be used. The drying operation may include a spin speed as high as 2,000 rpm.

[0021] While the cleaning operation of the present invention was described above in conjunction with a dielectric etching process, such is exemplary only and the cleaning operation of the present invention may be used at various stages during the manufacturing process used to form semiconductor devices.

[0022] The preceding merely illustrates the principles of the invention. It will thus be appreciated that those skilled in the art will be able to devise various arrangements which, although not explicitly described or shown herein, embody the principals of the invention and are included within its spirit and scope. Furthermore, all examples and conditional language recited herein are principally intended expressly to be only for pedagogical purposes and to aid the reader in understanding the principals of the invention and the concepts contributed by the inventors to furthering the art, and are to be construed as being without limitation to such specifically recited examples and

conditions. Moreover, all statements herein reciting principles, aspects, and embodiments of the invention, as well as specific examples thereof, are intended to encompass both structural and functional equivalents thereof. Additionally, it is intended that such equivalents include both currently known equivalents and
5 equivalents developed in the future, i.e., any elements developed that perform the same function, regardless of structure.

[0023] This description of the exemplary embodiments is intended to be read in connection with the accompanying drawings, which are to be considered part of the entire written description. In the description, relative terms such as "lower", "upper",
10 "horizontal", "vertical", "above", "below", "up", "down", "top" and "bottom" as well as derivative thereof (e.g., "horizontally", "downwardly", "upwardly", etc.) should be construed to refer to the orientation as then described or as shown in the drawing under discussion. These relative terms are for convenience of description and do not require that the apparatus be constructed or operated in a particular orientation. Terms
15 concerning attachments, coupling and the like, such as "connected" and "interconnected", refer to a relationship wherein structures are secured or attached to one another either directly or indirectly through intervening structures, as well as both movable or rigid attachments or relationships, unless expressly described otherwise.

[0024] Although the invention has been described in terms of exemplary
20 embodiments, it is not limited thereto. Rather, the appended claims should be construed broadly, to include other variants and embodiments of the invention, which may be made by those skilled in the art without departing from the scope and range of equivalents of the invention.